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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/593,912	06/14/2000	Yatin R. Acharya	E0897	8324

7590 07/21/2004

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EXAMINER	
YAO, KWANG BIN	
ART UNIT	**PAPER NUMBER**
2667	

DATE MAILED: 07/21/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/593,912	Applicant(s) ACHARYA, YATIN R.	
	Examiner Kwang B. Yao	Art Unit 2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 27-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-18, 27-34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-18, 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 5,809,026) in view of Quigley et al. (US 6,650,624).

Wong et al. discloses a communication system comprising the following features: as depicted in Fig. 2, regarding claim 1, a common bus (36a , 36b) port for electrical coupling to a common bus (36a , 36b) that is electrically coupled to the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f), the common bus (36a , 36b) serving as a direct interface between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f); and logical circuitry to transmit a data block from the common bus (36a , 36b) port to a respective one of the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f) by way of the common bus (36a , 36b); regarding claim 7, a processor coupled to a local interface; a common bus (36a , 36b) port coupled to the local interface, the common bus (36a , 36b) port being adapted for electrical

coupling to a common bus (36a , 36b) that is electrically coupled to the number of physical layer devices (24a, 24b, 24c ,24d, 24e, 24f), the common bus (36a , 36b) serving as a direct interface between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f): and logic to transmit a data block from the common bus (36a , 36b) port to a respective one of the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f) by way of the common bus (36a , 36b); regarding claim 13, a common bus (36a , 36b) port coupled to the local interface, the common bus (36a , 36b) port being adapted for electrical coupling to a common bus (36a , 36b) that is electrically coupled to the number of physical layer devices (24a, 24b, 24c ,24d, 24e, 24f), the common bus (36a , 36b) serving as a direct interface between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f); and means for transmitting a data block from the common bus (36a , 36b) port to a respective one of the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f) by way of the common bus (36a , 36b); regarding claim 16, the common bus (36a , 36b) serving as a direct interface between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f); regarding claim 27, wherein the electrical coupling includes a pin connection on an integrated circuit; regarding claim 28, wherein the electrical coupling includes a plug-in connection on an integrated circuit; regarding claim 29, wherein the electrical coupling includes a pin connection between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f) in a single integrated circuit; regarding claim 30, wherein the electrical coupling includes a connection on an integrated circuit; regarding claim 31, wherein the electrical coupling includes a plug-in connection on an integrated circuit; regarding claim 32, wherein the electrical coupling includes a connection between the media access controller (36) and the physical layer devices (24a, 24b,

24c ,24d, 24e, 24f) in a single integrated circuit; regarding claim 33, wherein the electrical coupling includes at least one of a pin connection on an integrated circuit, a plug-in connection on an integrated circuit and a connection between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f) in a single integrated circuit; regarding claim 34, wherein the electrical coupling includes at least one of a pin connection on an integrated circuit, a plug-in connection on w integrated circuit and a connection between the media access controller (36) and the physical layer devices (24a, 24b, 24c ,24d, 24e, 24f) in a single integrated circuit. See column 3-5.

Wong et al. does not disclose the following features: regarding claim 1, logical circuitry to transmit a training sequence front the common bus port to the physical layer devices; the data block being transmitted in one of a number of time slots of a time division multiplexed transmission; regarding claim 2, wherein the logical circuitry to transmit a training sequence from the common bus port further comprises logical circuitry to transmit a transmit enable signal froze the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices; regarding claim 3, wherein the logical circuitry to transmit a training sequence from the common bus port to the physical layer devices further comprises logical circuitry to transmit an address designation in each of the time slots; regarding claim 4, wherein the logical circuitry to transmit a training sequence from the common bus port to the physical layer devices further comprises logical circuitry to transmit a predefined training sequence that provides a reference for the time slots; regarding claim 5, , wherein each of the address designations is transmitted in a first portion of the corresponding time slot; regarding claim 6, wherein a predetermined sequence is transmitted in a second portion of the

corresponding time slot; regarding claim 7, a memory coupled to the local interface; and operating logic stored on the memory and executable by the processor, the operating logic further comprising: logic to transmit a training sequence from the common bus port to the physical layer devices; the data block being transmitted in one of a number of time slots of a time division multiplexed TDM transmission; regarding claim 8, the logic to transmit a training sequence from the common bus port to the physical layer devices further comprises logic to transmit a transmit enable signal from the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices; regarding claim 9, wherein the logic to transmit a training sequence from the common bas port to the physical layer devices further comprises logic to transmit an address designation in each of the time slots; regarding claim 10, wherein the logic to transmit a training sequence from the common bus port to the physical layer devices further comprises logic to transmit a predefined training sequence that provides a reference for the time slots; regarding claim 11, wherein each of the address designations is transmitted in a first portion of the corresponding time slot; regarding claim 12, wherein a predetermined sequence is transmitted in a second portion of the corresponding time slot; regarding claim 13, means for transmitting a training sequence from the common bus port to the physical layer devices; the data block being transmitted in one of a number of time slots of a time division multiplexed TDM transmission; regarding claim 14, wherein the means for transmitting a training sequence from the common bus port to the physical layer devices further comprises means for transmitting a transmit enable signal from the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices; regarding claim 15, means for transmitting a training sequence from the

common bus port to the physical layer devices further comprises means for transmitting an address designation in each of the time slots; regarding claim 16, transmitting a training sequence to the physical layer devices by way of a common bus; and transmitting a data block to a respective one of the physical layer devices by way of the common bus, the data block being transmitted in one of a number of time slots of a time division multiplexed TDM transmission; regarding claim 17, wherein the step of transmitting a training sequence to the physical layer devices by way of a common bus further comprises the step of transmitting a transmit enable signal to the physical layer devices by way of the common bus simultaneously with the transmission of the data block, thereby indicating a transmission of the data block to the physical layer devices; regarding claim 18, wherein the step of transmitting a training sequence to the physical layer devices by way of a common bus further comprises the step of transmitting an address designation in each of the time slots.

Quigley et al. discloses a communication system comprising the following features: as depicted in Figs. 34, 35, regarding claim 1, logical circuitry to transmit a training sequence (722) front the common bus port to the physical layer devices (332); the data block (723) being transmitted in one of a number of time slots (Figs. 43, 48, 49, 50, 51, 52, 53) of a time division multiplexed transmission; regarding claim 2, wherein the logical circuitry to transmit a training sequence (722) from the common bus port further comprises logical circuitry to transmit a transmit enable signal (Fig. 66, 602a, Fig. 67, 602b) from the common bus port simultaneously with the data block (723), thereby indicating a transmission of the data block (723) to the physical layer devices (332); regarding claim 3, wherein the logical circuitry to transmit a training sequence (722) from the common bus port to the physical layer devices (332) further

comprises logical circuitry to transmit an address designation in each of the time slots (Figs. 43, 48, 49, 50, 51, 52, 53); regarding claim 4, wherein the logical circuitry to transmit a training sequence (722) from the common bus port to the physical layer devices (332) further comprises logical circuitry to transmit a predefined training sequence (722) that provides a reference for the time slots (Figs. 43, 48, 49, 50, 51, 52, 53); regarding claim 5, , wherein each of the address designations is transmitted in a first portion of the corresponding time slot; regarding claim 6, wherein a predetermined sequence is transmitted in a second portion of the corresponding time slot; regarding claim 7, a memory coupled to the local interface; and operating logic stored on the memory and executable by the processor, the operating logic further comprising: logic to transmit a training sequence (722) from the common bus port to the physical layer devices (332); the data block (723) being transmitted in one of a number of time slots (Figs. 43, 48, 49, 50, 51, 52, 53) of a time division multiplexed TDM transmission; regarding claim 8, the logic to transmit a training sequence (722) from the common bus port to the physical layer devices (332) further comprises logic to transmit a transmit enable signal (Fig. 66, 602a, Fig. 67, 602b) from the common bus port simultaneously with the data block (723), thereby indicating a transmission of the data block (723) to the physical layer devices (332); regarding claim 9, wherein the logic to transmit a training sequence (722) from the common bas port to the physical layer devices (332) further comprises logic to transmit an address designation in each of the time slots (Figs. 43, 48, 49, 50, 51, 52, 53); regarding claim 10, wherein the logic to transmit a training sequence (722) from the common bus port to the physical layer devices (332) further comprises logic to transmit a predefined training sequence (722) that provides a reference for the time slots (Figs. 43, 48, 49, 50, 51, 52, 53); regarding claim 11, wherein each of the address designations is

transmitted in a first portion of the corresponding time slot; regarding claim 12, wherein a predetermined sequence is transmitted in a second portion of the corresponding time slot; regarding claim 13, means for transmitting a training sequence (722) from the common bus port to the physical layer devices (332); the data block (723) being transmitted in one of a number of time slots (Figs. 43, 48, 49, 50, 51, 52, 53) of a time division multiplexed TDM transmission; regarding claim 14, wherein the means for transmitting a training sequence (722) from the common bus port to the physical layer devices (332) further comprises means for transmitting a transmit enable signal (Fig. 66, 602a, Fig. 67, 602b) from the common bus port simultaneously with the data block (723), thereby indicating a transmission of the data block (723) to the physical layer devices (332); regarding claim 15, means for transmitting a training sequence (722) from the common bus port to the physical layer devices (332) further comprises means for transmitting an address designation in each of the time slots (Figs. 43, 48, 49, 50, 51, 52, 53); regarding claim 16, transmitting a training sequence (722) to the physical layer devices (332) by way of a common bus; and transmitting a data block (723) to a respective one of the physical layer devices (332) by way of the common bus, the data block (723) being transmitted in one of a number of time slots (Figs. 43, 48, 49, 50, 51, 52, 53) of a time division multiplexed TDM transmission; regarding claim 17, wherein the step of transmitting a training sequence (722) to the physical layer devices (332) by way of a common bus further comprises the step of transmitting a transmit enable signal (Fig. 66, 602a, Fig. 67, 602b) to the physical layer devices (332) by way of the common bus simultaneously with the transmission of the data block (723), thereby indicating a transmission of the data block (723) to the physical layer devices (332); regarding claim 18, wherein the step of transmitting a training sequence (722) to the physical

layer devices (332) by way of a common bus further comprises the step of transmitting an address designation in each of the time slots (Figs. 43, 48, 49, 50, 51, 52, 53). See column 42-74. It would have been obvious to one of the ordinary skill in the art the time of the invention to modify the system of Wong et al., by using the features, as taught by Quigley et al., in order to provide an efficient and reliable communication system. See Quigley et al., column 3, lines 23-32.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 703-308-7583. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H Pham can be reached on 703-305-4378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER
Kwang B. Yao
July 14, 2004